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Question Paper Code : X 60373

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Third Semester
Computer Science and Engineering
CS 2202/CS 34/EC 1206 A/080230012/10144 CS 303 – DIGITAL PRINCIPLES AND SYSTEM DESIGN
(Common to Information Technology)
(Regulations 2008/2010)
(Also common to PTCS 2202 – Digital Principles and System Design for B.E. (Part-Time) – Second Semester – CSE – Regulations 2009)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Convert the binary number 10111011 into gray code.
2. What is meant by duality in Boolean algebra ?
3. Implement a full adder with two half adders.
4. Implement a 4-bit even parity checker.
5. Draw the truth table and circuit diagram of 4 to 2 encoder.
6. Distinguish EEPROM and flash memory.
7. Derive the characteristic equation of a JK-flipflop.
8. What is a Mealy circuit ?
9. State One Hot State Assignment.
10. Compare the ASM chart with a conventional flowchart.

PART – B **(5×16=80 Marks)**

11. a) Simplify the following Boolean function using Quine-McClusky method $F = (A , B, C, D, E) = \sum m(0, 1, 3, 7, 13, 14, 21, 26, 28) + \sum d(2, 5, 9, 11, 17, 24)$. **(16)**

(OR)

b) i) Simplify the given Boolean function in POS form using K-map and draw the logic diagram using only NOR gates.

F(A , B, C, D) = πM(0, 1, 4, 7, 8, 10, 12, 15) + d(2, 6, 11, 14). **(10)**

ii) Convert 78.5_{10} into binary. **(3)**

iii) Find the dual and complement of the following Boolean expression xyz' + x' yz + z(xy + w). **(3)**

12. a) i) With the neat diagram, discuss the working principle of carry look-ahead adder. **(11)**

ii) Design a 4-bit adder using three full adders and one half adder. **(5)**

(OR)

b) i) Write the VHDL code for BCD-to-7 segment code convertors, using a selected signal assignment. **(12)**

ii) Write test bench for half adder circuit. **(4)**

13. a) i) Write notes on PLA and PAL. **(8)**

ii) Implement F(A, B, C, D) = ∑(1, 3, 4, 11, 12, 13, 14, 15) using 8 × 1 multiplexer. **(8)**

(OR)

b) i) Write notes on RAM, its operations and its types. **(10)**

ii) Design a 4-input priority encoder. **(6)**

14. a) Design a sequential circuit with two T-flip flops A and B, one input X and one output Z is specified by the following next state and output equation is

A (t + 1) = BX' + B'X

B (t + 1) = AB + BX + AX

Z = AX' + A'B'X

i) Draw the logic diagram of the circuit.

ii) List the state table for the sequential circuit.

iii) Draw the corresponding state diagram. **(16)**

(OR)

b) i) Draw and explain the parallel in serial out shift register and explain. **(8)**

ii) Draw the block diagram of Johnson counter and explain. **(8)**

15. a) i) Explain the types of hazards in digital circuits. **(6)**

ii) Implement the switching function F = ∑m(l, 3, 5, 7, 8, 9, 14,15) by a static hazard free 2 level AND-OR gate network. **(10)**

(OR)

b) Explain the steps for the design of asynchronous sequential circuits.

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